B022412(022)

B. Tech (Fourth Semester) Examination, April-May 2021

(Computer Science and Engg. Branch)

COMPUTER SYSTEM ARCHITECTURE

Time Allowed: Three hours

Maximum Marks: 100

Minimum Pass Marks: 35

Note: Attempt all question. Part (a) of all questions is compulsory. Attempt any two parts from (b), (c) and (d). The figure in the right-hand margin indicate marks.

Unit-I

- 1. (a) Who controls the buses in DMA data transfer and how?
 - (b) What do you understand by a subroutine? Discuss about parameter passing in subroutines.

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(c)	Write the differences between Hardwired and Micro
	programmed control unit. Draw the block diagram
	of both.

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(d) An instruction is stored at location 300 with its address field at location 301. The address field has the value 400, a processor register R1 contain the number 200. Evaluate effective address if the addressing mode of the instruction are

- (i) direct
- (ii) immediate
- (iii) relative
- (iv) register indirect

Unit-I

- 2. (a) In a computer with 48-bit words, one bit is reserved for the sign. What will be the range of fixed-point integer number?
 - (b) Describe a technique used to make the process of addition and subtraction by 2's complement number faster.
 - (c) Explain Booth multiplication alongwith for 2's complement number using flow chart and example. 8

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(d) Evaluate the following by using Restoring Division: Divisor is 11 and Divided is 1000.

Unit-III

- 3. (a) Define the principle of locality of references. Which parameter is used to evaluate the performance of cache memory?
 - (b) The access time of cache memory is 100 ns and that of main memory 1000 ns. It is estimated that 80% of the memory request for read and remaining for write. The hit ratio for read access only is 0.9. A write through procedure is used.
 - (i) What is the average access time of system considering only memory read?
 - (ii) What is the average access time of system for both read and write required?
 - (c) What do you mean by virtual memory? An address space is specified by 24 bits and corresponding memory space by 16 bits.
 - (i) How many word are there in the address space?
 - (ii) How many words are there in the memory space?
 - pages and blocks are there in the system?
 - (d) Explain the working of associative memory with

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	(7)	
	block diagram and derive the expression for match	
	logic. Course behand how that purpoint	8
	Unit-IV	
4.	(a) How Daisy Chaining priority interrupt works?	4
	(b) Explain the direct memory access scheme alongwith its advantages for data transfer between external devices and the main memory.	8
	(c) Explain in detail about the structure of a magnetic disk system. Also mention how we can find its capacity.	8
	(d) What do you understand by computer peripherals? Explain with proper explanation any two computer peripherals.	8
	Unit-V Resulting of Common Laurus of melin may a humilW [13]	
5.	(a) Specify a pipeline configuration to carry out	
	arithmetic operation $(A_i + B_i)(C_i + D_i)$	4
	(b) Consider the execution of the program 15000 instruction a linear pipeline processor with a clock rate of 25 MHz. Assume that the instruction pipeline	
	has 5 stages and that one instruction is issued per	

clock cycle. Calculate	8
(i) speed up factor	
(ii) efficiency	
(iii) throughout.	
(c) What do you understand by parallel processing?	
Describe Flynn's classification of parallel processing.	8
(d) What is the use of pipelining? Prove that an M-	
stage linear pipeline can be at most M times faster	
than that of non-pipelined serial processor.	8